We Claim:

1. A method for fabricating a semiconductor structure, which comprises:

providing a layer to be patterned at a semiconductor substrate;

providing a sacrificial layer between the layer to be patterned and a resist layer;

patterning the resist layer to form a patterned resist layer with depressions;

selectively etching the sacrificial layer with a taper angle in an etching direction to reduce dimensions within the sacrificial layer in the etching direction, the dimensions being prescribed by the depressions in the patterned resist layer; and

selectively etching the layer to be patterned utilizing the sacrificial layer, etched with the taper angle, as a mask.

2. The method according to claim 1, which further comprises selecting a resist material as the sacrificial layer.

3. The method according to claim 1, which further comprises providing an organic antireflection layer as the sacrificial layer.

4. The method according to claim 1, which further comprises selecting the layer to be patterned from the group consisting of a dielectric layer, a metal layer, and a polysilicon layer.

5. The method according to claim 1, which further comprises etching the layer to be patterned with the taper angle being between approximately 45 degrees and approximately 90 degrees.

6. The method according to claim 1, which further comprises etching the layer to be patterned with the taper angle being between approximately 70 degrees and approximately 85 degrees.

7. The method according to claim 1, which further comprises etching the layer to be patterned with the taper angle of approximately 80 degrees.

8. The method according to claim 1, which further comprises after etching the sacrificial layer with the taper angle, carrying out the selective etching of the layer step by patterning the layer to be patterned with depressions having dimensions no greater than approximately 180 nm.

9. The method according to claim 1, which further comprises after etching the sacrificial layer with the taper angle, carrying out the selective etching of the layer step by patterning the layer to be patterned with depressions having dimensions between approximately 55 nm and approximately 120 nm.

10. The method according to claim 1, which further comprises after etching the sacrificial layer with the taper angle, carrying out the selective etching of the layer step by patterning the layer to be patterned with depressions having dimensions no greater than approximately 180 nm.

11. The method according to claim 1, which further comprises after etching the sacrificial layer with the taper angle, carrying out the selective etching of the layer step by patterning the layer to be patterned with depressions having dimensions between approximately 55 nm and approximately 120 nm.

12. A method for fabricating a semiconductor structure, which comprises:

providing a layer to be patterned at a semiconductor substrate;

providing at least one sacrificial layer at the layer to be patterned;

providing a resist layer at the sacrificial layer to dispose the sacrificial layer between the resist layer and the layer to be patterned;

patterning the resist layer to form depressions therein, the depressions having dimensions;

selectively etching the sacrificial layer with a taper angle in an etching direction dependent upon the dimensions of the depressions to create an etched sacrificial layer having etching dimensions smaller than the dimensions of the depression; and

selectively etching the layer to be patterned using, as a mask, the etched sacrificial layer having the taper angle.

13. The method according to claim 12, which further comprises selecting a resist material as the sacrificial layer.

14. The method according to claim 12, which further comprises providing an organic antireflection layer as the sacrificial layer.

15. The method according to claim 12, which further comprises selecting the layer to be patterned from the group consisting of a dielectric layer, a metal layer, and a polysilicon layer.

16. The method according to claim 12, which further comprises etching the sacrificial layer with the taper angle being between approximately 45 degrees and approximately 90 degrees.

17. The method according to claim 12, which further comprises etching the sacrificial layer with the taper angle being between approximately 70 degrees and approximately 85 degrees.

18. The method according to claim 12, which further comprises etching the sacrificial layer with the taper angle of approximately 80 degrees.

19. The method according to claim 12, which further comprises after etching the sacrificial layer with the taper angle, carrying out the selective etching of the layer step by patterning the layer to be patterned with depressions having dimensions no greater than approximately 180 nm.

20. The method according to claim 12, which further comprises after etching the sacrificial layer with the taper angle, carrying out the selective etching of the layer step by patterning the layer to be patterned with depressions having

dimensions between approximately 55 nm and approximately 120 nm.

21. The method according to claim 12, which further comprises after etching the sacrificial layer with the taper angle, carrying out the selective etching of the layer step by patterning the layer to be patterned with depressions having dimensions no greater than approximately 180 nm.

22. The method according to claim 12, which further comprises after etching the sacrificial layer with the taper angle, carrying out the selective etching of the layer step by patterning the layer to be patterned with depressions having dimensions between approximately 55 nm and approximately 120 nm.

23. A method for fabricating a semiconductor structure, which comprises:

providing a layer to be patterned at a semiconductor substrate;

providing two sacrificial layers between the layer to be patterned and a resist layer with the first sacrificial layer disposed toward the resist layer and the second sacrificial layer being disposed toward the layer to be patterned;

patterning the resist layer to form a patterned resist layer with depressions;

selectively etching the first sacrificial layer with a taper angle in an etching direction to reduce dimensions within the first sacrificial layer, the dimensions being prescribed by the depressions in the patterned resist layer;

selectively etching the second sacrificial layer utilizing the first sacrificial layer, etched with the taper angle, as a mask; and

selectively etching the layer to be patterned utilizing the second etched sacrificial layer as a mask.

24. The method according to claim 23, which further comprises selecting the first sacrificial layer from the group consisting of a dielectric layer, a polysilicon layer, and a metal layer.

25. The method according to claim 24, which further comprises selecting the dielectric layer from the group consisting of silicon oxide, silicon oxynitride, and silicon nitride.

26. The method according to claim 23, which further comprises selecting a resist material as the second sacrificial layer.

27. The method according to claim 26, which further comprises selecting the resist material from the group consisting of an organic antireflection layer and a layer having carbon as the main constituent.

28. The method according to claim 23, which further comprises selecting a carbon layer as the second sacrificial layer.

29. The method according to claim 23, which further comprises:

carrying out the first sacrificial layer etching step by etching substantially only the first sacrificial layer with the taper angle to reduce the dimensions within the first sacrificial layer, the dimensions being prescribed by the depressions in the patterned resist layer; and

carrying out the second sacrificial layer etching step by etching the second sacrificial layer substantially with straight edges.

30. The method according to claim 23, which further comprises selecting the layer to be patterned from the group consisting of a dielectric layer, a metal layer, and a silicon layer.

31. The method according to claim 30, which further comprises selecting silicon oxide as the dielectric layer.

32. The method according to claim 23, which further comprises selecting:

a polysilicon layer as the first sacrificial layer;

one of the group consisting of silicon oxide and silicon oxynitride as the second sacrificial layer; and

a metal layer as the layer to be patterned.

33. The method according to claim 24, which further comprises selecting:

a polysilicon layer as the first sacrificial layer;

one of the group consisting of silicon oxide and silicon oxynitride as the second sacrificial layer; and

a metal layer as the layer to be patterned.

34. The method according to claim 30, which further comprises selecting:

a polysilicon layer as the first sacrificial layer;

one of the group consisting of silicon oxide and silicon oxynitride as the second sacrificial layer; and

a metal layer as the layer to be patterned.

35. The method according to claim 23, which further comprises etching first sacrificial layer with the taper angle being between approximately 45 degrees and approximately 90 degrees.

36. The method according to claim 23, which further comprises etching first sacrificial layer with the taper angle being between approximately 70 degrees and approximately 85 degrees.

37. The method according to claim 23, which further comprises etching first sacrificial layer with the taper angle of approximately 80 degrees.

38. The method according to claim 23, which further comprises after etching the first sacrificial layer with the taper angle, carrying out the selective etching of the layer step by

at least one of patterning the layer to be patterned and etching the second sacrificial layer with depressions having dimensions no greater than approximately 180 nm.

39. The method according to claim 23, which further comprises after etching the first sacrificial layer with the taper angle, carrying out the selective etching of the layer step by at least one of patterning the layer to be patterned and etching the second sacrificial layer with depressions having dimensions between approximately 55 nm and approximately 120 nm.

40. A method for fabricating a semiconductor structure, which comprises:

providing a layer to be patterned at a semiconductor substrate;

providing at least two sacrificial layers at the layer to be patterned with the second sacrificial layer being disposed toward the layer to be patterned and the first sacrificial layer disposed away from the layer to be patterned;

providing a resist layer at the first sacrificial layer to dispose the first sacrificial layer between the resist layer and the second sacrificial layer;

patterning the resist layer to form depressions therein, the depressions having dimensions;

selectively etching the first sacrificial layer with a taper angle in an etching direction dependent upon the dimensions of the depressions to create an etched first sacrificial layer having etching dimensions smaller than the dimensions of the depressions;

selectively etching the second sacrificial layer utilizing the first sacrificial layer, etched with the taper angle, as a mask; and

selectively etching the layer to be patterned utilizing, as a mask, the second etched sacrificial layer.